Remarks:

Reconsideration of the application is requested.

Claims 1-6 remain in the application. Claims 1, 3, and 5 have been amended.

In item 3 on page 2 of the Office action, claims 1, 2, 5, and 6 have been rejected as being obvious over Applicant's admitted prior art in view of Ugajin et al. (JP 363292747 A) under 35 U.S.C. § 103.

The Examiner's determination of the teaching of JP 363292747 A goes far beyond what applicant has discerned from reviewing the English language abstract. The Examiner has cited portions on pages 281 and 282 of JP 363292747 A, which leads one to believe that the Examiner is in possession of a translation of the entire document. If the Examiner is in possession of a translation of the entire document or at least of major portions thereof, applicant requests that a copy of the translation be provided.

Claims 1, 3, and 5 have been amended to better define the invention. Support for the changes to the claims can be found by referring to the application at page 11, lines 7-22, for example. The claimed invention now relates to an ISDN-data

transmission method for transmitting digital data divided up into HDLC data frames of variable lengths.

The portions of the claims that have been underlined below relate to the Examiner's argumentaion.

Claim 1 defines an improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus to a second data bus operated asynchronously with respect to the first data bus and controlled by a microprocessor. The method includes steps of:

writing the digital data from the first data bus to a memory having a settable size;

informing the microprocessor, in a form of an interrupt generated by a memory control unit, if the memory is full or an end of a data frame has been reached;

determining via the microprocessor from the memory control unit a quantity of the digital data to be read from the memory;

reading via the microprocessor the digital data from the memory;

setting via the microprocessor a size of the memory; and

transmitting from the microprocessor to the memory control unit an acknowledgment of a reception of a data block of the digital data.

Claim 5 defines a configuration for performing an ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable length from a first data bus to a second data bus operated asynchronously with respect to the first data bus and controlled and read by a microprocessor. The configuration includes:

a memory having a variable size for storing data received from the first data bus;

a control device for controlling access operations to said memory by the first data bus and the microprocessor;

a first register storing a value representing a present size of said memory, said value being variable in each read cycle of the microprocessor; and

a second register storing a quantity of the data just written to said memory.

The Examiner has the opinion that the prior art timing diagrams shown in Figs 6A and 6B of the application disclose the claimed invention except for the portions that have been underlined above. The Examiner then, however, has the opinion that the underlined portions of the claims are known from JP 363292747 A and that it would have been obvious to combine the teachings to arrive at the invention defined by claims 1, and 5.

Applicant believes that one does not obtain a suggestion to incorporate the features that are not taught in Figs 6A and 6B merely by referring to JP 363292747 A.

Claims 1 and 5 respectively define a method and a configuration for ISDN data transmission, in which the size of the intermediate storage is adapted to the HDLC data packets that will be transmitted for the purpose of efficient and rapid data communication. An adaptation of a memory, as indicated, for example, in JP 363292747 A, represents a commonly known measure, as was correctly stated by the Examiner, however one of ordinary skill in the art - based on this knowledge - does not get to the method defined by claim 1 or to the configuration defined by claim 5. Instead, for data communication according to the ISDN standard (or according to the instant application), the correspondingly adjustable memory would have to be suitable to be adapted to this

standard. This, however, requires additional adaptation steps that would not be possible without an inventive teaching that is missing from the prior art. Particularly, the adjustable memory would also have to be designed for the transmission of the fixed data packets, as they are common in ISDN standard.

JP 363292747 A, however, does not give any information with regard thereto. This document discloses a buffer memory device with a memory size that can be variably adjusted. JP 363292747 A merely describes variably partitioning an intermediate storage device between a transmission device and a reception device.

Contrary thereto, the claimed invention relates to an intermediate storage device that is able to receive data packets, so-called HDLC frames, with a variable length. The novel aspect thereby is that the size of the FIFO memory, as opposed to the read-out microcontroller, can be dynamically adjusted between two reading operations of the microcontroller. The particular advantage herein is that the microcontroller is able to adjust the size of the intermediate storage device that will be read by the microcontroller, i.e., dependent on the content of the HDLC frame that is written on the respective other side of the intermediate storage precisely at this moment.

However, none of the text passages of JP 363292747 A disclose whether the intermediate storage device is structured in a variable manner. An intermediate storage device according to JP 363292747 A for constantly structured data or even blocks of constant size, as for example in ATM systems, however, can be realized in a much simpler manner, than an intermediate storage device that must also manage data, for example, information regarding the beginning and the end of an HDLC frame.

JP 363292747 A obviously pertains to a data transmission system that is similar to the ATM system. This system, in which data frames of constant length are provided (for example 53 Bytes) was already standardized, in particular due to the fact that the intermediate storage can be realized in a much simpler manner than if the data frames were to have variable lengths.

In summary one of ordinary skill in the art would not combine JP 363292747 A with the prior art discussed in the application, because JP 363292747 A is simply not pertinent.

In item 4 on page 5 of the Office action, claims 3 and 4 have been rejected as being obvious over Applicant's admitted prior art in view of Ugajin et al. (JP 363292747 A) and Chee et al.

(5,673,416) under 35 U.S.C. § 103. Applicant respectively traverses.

Claim 3 defines an improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus, controlled by a microprocessor, to a second data bus operated asynchronously with respect to the first data bus, the improvement which comprises:

writing the digital data from the first data bus to a memory having a settable size;

performing one of informing the microprocessor, in a form of an interrupt generated by a memory control unit, if the memory is ready to accept new data from the first data bus, and the microprocessor asking the memory control unit if the memory is ready to accept the new data from the first data bus;

writing via the microprocessor the new data to the memory;

setting via the microprocessor a size of the memory;

transmitting from the microprocessor to the memory control unit an acknowledgment of an end of transmission of the new data; and

placing the new data onto the second data bus.

Claim 3 is not obvious for the reasons specified above with regard to JP 363292747 A.

Further, applicant believes that Chee et al. (5,673,416) is not relevant in view of the object of the instant application. Chee et al. describe a FIFO memory with a low and a high threshold. The low threshold of the FIFO has sufficient storage space for new data. The high threshold is used when the FIFO memory must be filled in order to prevent a so-called "underrun". The instant application, to the contrary, has a single priority, i.e. an intermediate storage device that manages data frames of variable lengths and that is adapted to the content of the data. The content herein describes the length of the frame, and the beginning and the end of the frame. Chee et al. is an intermediate storage device, the size of which is adjusted dependent on the amount of data that is coupled in or on the fill level of the FIFO memory. Data management, however, does not take place here.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 3, or 5. Claims 1, 3 and 5 are, therefore, believed to be patentable over the art

and since all of the dependent claims are ultimately dependent on claims 1, 3, or 5, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-6 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, he is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

Petition for extension is herewith made. The extension fee for response within a period of two-months pursuant to Section 1.136(a) in the amount of $410.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant

MPW:cgm

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